REMARKS

Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

This amendment revises independent claims 19 and 27 for clarity and to highlight patentable aspects of this invention.

In the final office action of September 23, 2005, claims 19-30 were rejected under 35 USC 103(a) as being unpatentable over Bussgang et al.

The Applicants respectfully traverse and submit that the amended claims are allowable over Bussgang et al., for at least the following reasons.

According to amended claim 19, the present invention includes the features of (1) a converting section that receives, through different routes, first and second information sequences each comprising plural bits in series and that divides each of the first information sequence and the second information sequence so as to generate a sequence of bits including at least one bit of the first information sequence and at least one bit of the second information sequence and (2) a bit corresponding to the first information sequence is arranged on at least the first bit of each of the symbols, and bits corresponding to the first information sequence are arranged on both the first bit and the second bit of at least one of the symbols. The above-noted features are supported by the

S/P converters 301, 302 of Fig. 3 and the accompanying specification description.

The final office action states that in Bussgang et al., each output line of the parallel-to-series converter 12 would include a sequence of a plurality of successive bits in series, and, for example, the first output line of the parallel-to-series converter would be X01, X02, X03, etc. (The Applicants note that in this same sense, the output of A/D converter 10 constitutes "parallel generated information bits, as signified by lines 11" (see col. 3, lines 35-36), and the bits on each output line constitute a serial sequence in the same sense that each output line of parallel-to-series converter 12 comprises a serial sequence of bits.)

With respect to the example proposed in the office action, bits X01, X02 and X03 are bits of successive samples, and each of the successive samples is digitized respectively by A/D converter 10 and received respectively by the parallel-to-series converter 12. For example, sequence X01, X02, X03 is always input to the first input of element 13, and sequence X11, X12 ,X13 is always input to the first input of element 14. X01 is combined with other bits of the sample to which it belongs, and output from element 13, and likewise for X02 and X03.

From the above, it is apparent that a plurality of bits in series in Bussgang et al. comprise a plurality of bits of successive samples.

In contrast, the plurality of bits in series recited in Applicants' claim 19 is comprised of one sample (either the first information sequence or the second information sequence), and the converting section divides the one sample so as to generate a serial sequence including bits of a plurality of samples.

With respect to the feature of amended claim 19 that, "bits corresponding to the first information sequence are arranged on both the first bit and the second bit of at least one of the symbols," it is submitted that such feature is not disclosed or suggested by Bussgang et al. as will be apparent from the following points.

In Bussgang et al., the first information sequence is comprised of a plurality of samples (e.g. X01, X02, etc.), the second information sequence is comprised of a plurality of samples (e.g. X11, X12, etc.), and likewise for the third through eighth sequences. Also, in Bussgang et al., a sequence of bits of a symbol is made from the bits of a single sample. That is, in Bussgang et al., bits of one information sequence (e.g., the first information sequence or the second information sequence) can not provide a

plurality of bits to one symbol; that is, a symbol can comprise only a single bit from each information sequence.

The above-noted feature ("bits corresponding to the first information sequence are arranged on both the first bit and the second bit of at least one of the symbols") that is added herein to the independent claims was recited in previous claim 21. The final office action rejected claim 21 on the grounds that it would have been obvious to arrange another bit of the first information sequence on the second bit of each symbol since Bussgang et al. stated that the first and second bit positions in the symbol afforded the greatest protection from error.

However, according to the interpretation proposed in the final office action of a sequence of bits in series in Bussgang et al., the first information sequence of Bussgang et al. (e.g. X01, X02, etc.) is comprised of bits to be arranged on only the first bit of a symbol output from element 13. Likewise, bit sequence X11, X12, etc. is comprised of bits to be arranged on only the first bit of a symbol output from element 14. Bit sequence X21, X22, etc. is comprised of bits to be arranged on only the second bit of a symbol. It is apparent that each of the bit sequences can be arranged on only one bit position of a symbol. Therefore, the rejection against claim 21 is impossible given the interpretation

of the first information sequence set forth in the final office action.

Further, since the bits of the first information sequence of Bussgang are to be arranged on only the first bit of a symbol, it is not necessary to divide the first information sequence at the converter (P/S converter 12). That is, the sequence is not divided through the converter.

In contrast, in the present claimed invention, the first and second information sequences are divided at the converter (converting section) so as to generate a sequence including a bit of the first information sequence and a bit of the second information sequence and a bit corresponding to the first information sequence is arranged on at least the first bit of each of the symbols, and bits corresponding to the first information sequence are arranged on both the first bit and the second bit of at least one of the symbols.

Accordingly, the Applicants respectfully submit that claim 19 and all claims dependent therefrom patentably distinguish over Bussgang et al.

Method claim 27 recites similar subject matter to that of claim 19, although in a method format. The Applicants respectfully submit that this claim, and all claims dependent therefrom, are

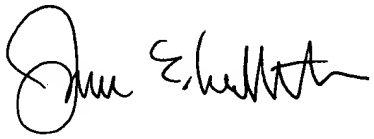
allowable over Bussgang et al. for similar reasons to those presented above for the allowance of claim 19.

For at least the above reasons, it is submitted that all of the present claims are allowable over the teachings of Bussgang et al.

In light of the foregoing, a notice of allowance is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the examiner is requested to telephone the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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